Customer No. 22,852
Attorney Docket No. 04329.3299

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Tsutomu SATO et al.	)	
	)	Group Art Unit:
Application No.: Not Yet Assigned	)	
	)	Examiner:
Filed: April 8, 2004	)	
	)	
For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	)	

MAIL STOP PATENT APPLICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§1.56 and 1.97(b), applicants bring to the Examiner's attention the documents listed on attached Form PTO-1449. Copies of the listed documents are attached. Applicants respectfully request that the Examiner consider the documents listed on attached Form PTO-1449 and indicate that they were considered by making an appropriate notation on this form.

This Information Disclosure Statement is being filed with the above-referenced application.

The following are listed on the accompanying PTO-1449 and are in a non-English language:

1. T. Sato et al., "A New Substrate Engineering for the Formation of Empty Space in Silicon (ESS) induced by Silicon Surface Migration", IEDM Technical Digest, pp. 517-520, (1999), discloses transforming the trench structure using silicon surface migration and presents how to make ESS.

2. T. Sato et al., "Discussion about dissolution of COP Defects by Direct Observation of Intentionally Grown Large Vacancy", Japan Society of Applied Physics, Extended Abstracts (The 60th Autumn Meeting, 1999), 2p-S-17, p. 355, (1999), discloses transforming the trench structure using silicon surface migration.

3. T. Sato et al., "ESS(Empty Space in Silicon) SON(Silicon on Nothing). A New Substrate Engineering using Silicon Surface Migration(1) SON Structure realized by ESS", Japan Society of Applied Physics, Extended Abstracts (The 47th Spring Meeting, 2000), 31a-YK-6, p. 888, (2000), discloses transforming the trench structure using silicon surface migration, and presents how to make ESS and theoretical study for ESS.

4. T. Sato et al., "ESS(Empty Space in Silicon). A New Substrate Engineering using Silicon Surface Migration(2) Design Guide for ESS Fabrication", Japan Society of Applied Physics, Extended Abstracts (The 47th Spring Meeting, 2000), 31a-YK-7, p. 889, (2000), discloses transforming the trench structure using silicon surface migration, and presents how to make ESS and theoretical study for ESS.

5. T. Sato et al., "Theoretical Study on the Formation Process of Empty Space in Silicon", Japan Society of Applied Physics, Extended Abstracts (The 47th Spring Meeting, 2000), 31a-YK-8, p. 889, (2000), discloses transforming the trench

structure using silicon surface migration, and presents how to make ESS and theoretical study for ESS.

6. T. Sato et al., "ESS(Empty Space in Silicon) SON(Silicon on Nothing). A New Substrate Engineering for the Formation of Empty Space in Silicon (ESS) induced by Silicon Surface Migration", Japan Society of Applied Physics, Silicon Technology, No. 14, pp. 61-65. (2000), discloses transforming the trench structure using silicon surface migration.

7. I. Mizushima et al., The Surface Science Society of Japan, 19th, p. 14, (1999), discloses structural transformation using silicon surface migration.

8. Japanese patent application publication no. 2000-58780, discloses rounding the corner of STI structure using silicon surface migration. An English language abstract of this document is enclosed.

9. Japanese patent application publication no. 10-256362, discloses making the void layer using hydrogen annealing. An English language abstract of this document is enclosed.

10. Japanese patent application publication no. 2000-12858, discloses the forming of a SON structure. The relevance of this document is discussed at pages 2, 3, 10, and 23 of the specification of the present application. An English language abstract of this document is also enclosed.

11. Japanese patent application publication no. 2001-257358, discloses a double gate MOSFET fabricated using SON structure, (Fig. 4). An English language abstract of this document is enclosed.

12. Japanese patent application publication no. 2001-144276, discloses that a SON structure was fabricated and the vacancy was filled with SiO2, (Fig. 6). The relevance of this document is discussed at pages 10 and 24 of the specification of the present application. An English language abstract of this document is also enclosed.

13. Japanese patent application publication no. 2002-324836, discloses that a SON structure was fabricated and the initial shape of the trench has low aspect ratio. An English language abstract of this document is enclosed.

14. Japanese patent application publication no. 2-280381, discloses a modified SOI transistor, (Fig. 1). An English language abstract of this document is enclosed.

15. Japanese patent application publication no. 60-150644, discloses vacancy exists partially under active device region, (Fig. 3). An English language abstract of this document is enclosed.

16. Japanese patent application publication no. 63-278375, discloses a transistor on vacancy, (Fig. 1). An English language abstract of this document is enclosed.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed

documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicants determine that the cited documents do not constitute "prior art" under United States law, applicants reserve the right to present to the Office the relevant facts and law regarding the appropriate status of such documents. Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: April 8, 2004

By: _____
Richard V. Burgujian
Reg. No. 31,744

Enclosures
RVB/FPD/blc

OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	04329.3299	Application No.	
Applicants	Tsutomu SATO et al.		
Filing Date	April 8, 2004	Group:	

U.S. PATENT DOCUMENTS							
Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
		6,570,217	May 27, 2003	T. Sato et al.			
		6,100,132	August 8, 2000	T. Sato et al.			
		6,552,380	April 22, 2003	T. Sato et al.			

FOREIGN PATENT DOCUMENTS							
		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
		2000-58780	February 25, 2000	Japan			Abstract
		10-256362	September 25, 1998	Japan			Abstract
		2000-12858	January 14, 2000	Japan			Abstract
		2001-257358	September 21, 2001	Japan			Abstract
		2001-144276	May 25, 2001	Japan			Abstract
		2002-324836	November 8, 2002	Japan			Abstract
		2-280381	November 16, 1990	Japan			Abstract
		60-150644	August 8, 1985	Japan			Abstract
		63-278375	November 16, 1988	Japan			Abstract

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	T. Sato et al., "A New Substrate Engineering for the Formation of Empty Space in Silicon (ESS) induced by Silicon Surface Migration", IEDM Technical Digest, pp. 517-520, (1999)
	T. Sato et al., "SON(Silicon on Nothing) MOSFET using ESS(Empty Space in Silicon) Technique for SoC Applications", IEDM Technical Digest, pp. 809-812, (2001)
	T. Sato et al., "ESS(Empty Space in Silicon) SON(Silicon on Nothing). A New Substrate Engineering for the Formation of Empty Space in Silicon (ESS) induced by Silicon Surface Migration", Japan Society of Applied Physics, Silicon Technology, No. 14, pp. 61-65. (2000)
	T. Sato et al., "Trench Transformation Technology using Hydrogen Annealing for Realizing Highly Reliable Device Structure with Thin Dielectric Films", 1998 Symposium on VLSI Technology, Digest of Technical Papers, pp. 206-207, (1988)
	S. Matsuda et al., "Novel Corner Rounding Process for Shallow Trench Isolation utilizing MSTS (Micro-Structure Transformation of Silicon)", IEDM Technical Digest, pp. 137-140, (1998)

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	I. Mizushima et al., The Surface Science Society of Japan, 19th, p. 14, (1999)
	M. Kito et al., "Semiconductor Device and Manufacturing Method Thereof", U.S. appln. no. 09/549,513, filed April 14, 2000
	T. Sato et al., "Semiconductor Substrate and its Fabrication Method", U.S. appln. no. 09/650,748, filed August 30, 2000
	A. Yagishita, "Semiconductor Device and Manufacturing Method Thereof", U.S. appln. no. 10/436,181, filed May 13, 2003
	K. Inoh, "Semiconductor Device with a Cavity therein and a Method of Manufacturing the same", U.S. appln. no. 10/665,614, filed September 19, 2003

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce